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REMARKS

Claims 1-6 and 8-21 are pending in which claim 7 is canceled herein. In the Office Action, the drawings were objected to as not showing every feature specified in the claims, the disclosure was objected to because of missing serial numbers of related applications, claims 4 and 5 were objected to because of informalities, and claims 1-8, 10-11, and 13-21 were rejected under 35 U.S.C. §102(b) as being anticipated by US Pat. No. 5,955,894 to Vishwanthaiah et al. (hereinafter "Vishwanthaiah").

The drawings were objected to as not showing the "clock signal" recited in claims 6, 16 and 19, and corrected drawing sheets were said to be required in reply to the Office Action to avoid abandonment.

Applicant respectfully traverses this objection to the drawings and the requirement of corrected drawing sheets since a clock signal is shown in the drawings and described in the written description. Applicant respectfully submits that no new drawings are necessary. FIGs 1 and 2 include a clock signal INT BCLK provided to the impedance controller 201 of the impedance matching logic 103. Paragraphs [0024], [0030] and [0031] describe the INT BCLK clock signal shown in the drawings. For example, paragraph [0024] introduces the clock signal and states that the impedance is determined or otherwise updated on selected cycles of INT BCLK, which is described as a "bus clock". In paragraph [0030] the impedance control logic 205 is a digital circuit controlled by the INT BCLK signal in which the SUM value is adjusted (incremented or decremented) during selected cycles of the clock signal.

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Claims 6, 16 and 19 recite “impedance control logic” receiving a clock signal. In claim 6, the reference impedance control input is incremented or decremented during selected cycles of the clock signal. In a similar manner, claim 16 recites a “reference impedance control input comprising a digital value, wherein said impedance control logic receives a clock signal and increments or decrements said reference impedance control input during selected cycles of said clock signal.” Further, claim 19 recites “incrementing or decrementing a digital value during selected cycles of a clock signal.” Applicant respectfully submits, therefore, that the clock signal is shown in the drawings and that the claims are clearly supported by the specification including the drawings and written description. Applicant requests withdrawal of this objection to the drawings and the requirement of corrected drawing sheets.

The Disclosure was objected to because of the missing serial numbers of the related applications listed in the table in paragraph [0002] on page 1. The Specification is amended to replace paragraph [0002] in its entirety in which the missing serial numbers are included. Applicant respectfully requests approval of this amendment and withdrawal of this objection.

Claim 4 was objected to because of antecedent basis for “the reference device.” Claim 4 is amended to replace the word “the” with “a” to properly introduce a reference device. Applicant respectfully submits that this objection has been overcome and requests withdrawal of this objection.

Claim 5 was objected to because of antecedent basis for “the reference value.” Applicant respectfully traverses this objection since antecedent basis is provided in the

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preamble of claim 1, which recites “[a]n impedance controller that controls termination impedance of at least one output based on *a reference value*” (emphasis added). Nonetheless, claim 5 is amended to replace “value” with “device” in reference to the reference device introduced in claim 4, upon which claim 5 depends. Applicant respectfully requests withdrawal of this objection.

Applicant respectfully traverses the §102(b) rejection of claims 2, 7-8, 11, 13, 20 and 21 as being anticipated by Vishwanthaiah.

Vishwanthaiah does not show or suggest a binary array of P-channel devices as recited in claims 2 and 13. The bit elements 210 and 212, 220 and 222, 404 and 504 of Vishwanthaiah each form a linear array rather than a binary array. As shown in FIG. 3 and as described in paragraphs [0032] – [0033] of the present application as filed, a binary array of devices means that the devices are binarily grouped (page 17, lines 4-6). As shown in FIG. 3, the devices are grouped in binary progression based on 2^N for $N = 0, 1, 2, \dots$, etc., (e.g., 1, 2, 4, 8, 16, etc.). In particular, the first “group” includes 1 device P1, the second group 301 includes 2 devices P3:P2, the third group 303 includes 4 devices P7:P4, the fifth group 305 includes 8 devices P15:P8, the sixth group 307 includes 16 devices P31:P16, and the seventh group 309 includes 32 devices P63:P32. Applicant respectfully submits, therefore, that claims 2 and 13 are allowable over Vishwanthaiah and requests withdrawal of this rejection.

Vishwanthaiah does not show or suggest “bias adjustment logic that combines a bias amount with said reference impedance control input to provide said termination impedance control input” as recited in claim 7. In the Office Action, it was stated that the

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claimed bias adjustment logic is met by element 540 in Vishwanthaiah. In Vishwanthaiah, a linear array of D-type flip-flops 540 form a register circuit 502. Each flip-flop 540 of the register circuit 540 has its D input coupled to a respective bit of a shift circuit 506, its Q output providing a respective one of a set of control bits (CNT BIT n , where n is an index from 1 to 8), and its clock input receiving a clock signal from a control circuit 510. If, according to the logic in the Office Action, the bits of the shift register are said to be providing a reference impedance control input to the register circuit 502, then the outputs of the register circuit 502 provide the termination impedance control input. Yet the register circuit 502 simply latches its inputs to its output without further modification, so that the reference impedance control input and the termination impedance control input are substantially the same (after being clocked) without further adjustment. There is no “bias amount” in Vishwanthaiah which is combined with a reference impedance control input by the register circuit 502 to provide a termination impedance control input.

It was further stated in the Office Action that Vishwanthaiah discloses “output bias logic” 510 that is programmed to provide a bias amount in reference to claim 8. Claim 8 recites “output bias logic that is programmed to provide said bias amount.” In Vishwanthaiah, element 510 is not bias logic but instead is described as a “control circuit” 510. There is no further description of the operation of the control circuit 510. By analogy, however, the control circuit 510 of FIG. 5 for controlling the pull-up devices is analogous in configuration and operation as the control circuit 410 of FIG. 4 for the pull-down devices. In Vishwanthaiah (col. 8, lines 4-34), the operation of control circuit 410 is described in further detail, in which it is stated that the control circuit 410

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“interprets and reacts to the sequence of output of the comparator 408.” And it is stated that the “nature of this sequence reflects whether or not the output impedance of bit element circuit 404 is close to the desired impedance.” And Vishwanthaiah then describes that if the output of the comparator 408 is switching every clock edge, “then the output resistance of circuit 404 is toggling on every clock edge between being just above and just below that of the external resistor.” Otherwise, the output of the comparator is the same for successive clock cycles. And Vishwanthaiah further states that the control circuit 410 provides a latch signal upon receiving the appropriate sequence from the comparator 408. FIG. 6 is shown an example of the control circuit 410 which achieves the desired function, which latches “when the output resistance of bit element circuit 404 is just less than that of resistor 122.” And FIG. 6 shows, once again, nothing more than a D-type flip-flop which is not programmable to provide a bias amount. Although there is no description of the operation of control circuit 510, it appears to operate in substantially the same manner as the control circuit 410.

In summary, the control circuits shown and describe in Vishwanthaiah simply operate to latch the appropriate value when the resistance of the bit element circuit substantially equals the resistance of the external reference resistor. There is no discussion whatsoever in Vishwanthaiah of bias amount or of any bias adjustment logic that combines a bias (or any other adjustment) with the reference value.

In contrast, the application as filed illustrates an exemplary embodiment of the claimed bias adjustment logic, although it is understood that Applicant’s claims are not limited to the particular embodiments disclosed in the application. FIG. 1 shows output bias logic 109 and paragraphs [0025] and [0026] describe the operation of the output bias

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logic 109. In particular, the output bias logic 109 is provided to add or subtract (based on control signal PSUBEN) a bias value PADD[3:0] to the PSUM[5:0] value. FIG. 2 shows the PSUBEN, PADD[3:0] and INT BCLK signals provided to bias adjust logic 209, which is described in paragraph [0031] of the application as filed. In particular, during selected cycles of INT BCLK, the bias adjustment logic 209 adjusts (e.g., increases or decreases) the PSUM[5:0] value based on the PADD[3:0] value and the control signal PSUBEN. And it is further stated that the PSUM[5:0] value is a "bias-adjusted version of the SUM[5:0] value." The bias amount may be determined by a test procedure or the like on a part-by-part basis, and may be programmed in any suitable manner, such as by a set of fuses or the like. And it is stated that the bias logic is a control mechanism that "enables a designer to compensate for process variations across the IC." No such bias functionality is shown or described in Vishwanthaiah.

Applicant respectfully submits, therefore, that claim 7 is allowable over Vishwanthaiah and requests withdrawal of this rejection. The substance of claim 7 is incorporated into claim 1 and claim 7 is canceled herein. Claim 8 is amended to depend on claim 1 rather than canceled claim 7. Applicant respectfully submits, therefore, that claims 1-8 are allowable over Vishwanthaiah and requests withdrawal of these rejections.

In a similar manner, Vishwanthaiah does not show or describe output bias logic that provides an adjustment value as recited in claim 11. Claim 10 is amended to include the output bias logic that provides an adjustment value, which is the same as that deleted from claim 11. And claim 10 is further amended to state that the "output termination logic that controls said termination impedance control input based on said reference impedance control input and said adjustment value." Applicant respectfully submits,

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therefore, that claims 10, 11 and 13-16 are allowable over Vishwanthaiah and requests withdrawal of this rejection.

In a similar manner, Vishwanthaiah does not show or describe a method of controlling pull-up termination impedance of at least one output based on a reference resistance, where the method includes programming a bias adjust value and controlling a termination impedance input based on a reference impedance input and the bias adjust value as recited in claim 20. This clause is deleted from claim 20 and incorporated into claim 17, which further recites “controlling a termination impedance input of at least one pull-up impedance generator based on the reference impedance input *and the bias adjust value*, wherein each pull-up impedance generator is coupled to a corresponding output” (emphasis added). Applicant respectfully submits that claims 17-21 are allowable over Vishwanthaiah and requests withdrawal of this rejection.

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CONCLUSION

Applicant respectfully submits that for the reasons recited above and for various other reasons, the objections and rejections have been overcome and should be withdrawn. Applicant respectfully submits therefore that the present application is in a condition for allowance and reconsideration is respectfully requested. Should this response be considered inadequate or non-responsive for any reason, or should the Examiner have any questions, comments or suggestions that would expedite the prosecution of the present case to allowance, Applicants' undersigned representative earnestly requests a telephone conference.

Respectfully submitted,

Date: July 26, 2005

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